(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 261 241 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.11.2002 Bulletin 2002/48

(51) Int Cl.[7]: **H05K 1/18**, H01C 7/00

(21) Application number: **02253403.6**

(22) Date of filing: **15.05.2002**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **17.05.2001 US 291353 P**

(71) Applicant: **Shipley Co. L.L.C.**
Marlborough, MA 01752 (US)

(72) Inventors:
- **Schemenaur, John**
  Tustin, California 92780 (US)
- **Senk, David D.**
  Mission Viejo, California 92692 (US)

(74) Representative: **Kent, Venetia Katherine**
Rohm and Haas (UK) Ltd
European Operations Patent Dept.
Lennig House
2 Mason's Avenue
Croydon, CR9 3NB (GB)

(54) Resistor and printed wiring board embedding those resistor

(57) Resistors having a resistive material portion including multiple layers or resistive materials, wherein each layer of resistive material has a different sheet resistivity, are provided by the present invention. Such resistors are particularly useful as embedded resistors in the manufacture of printed wiring boards. Methods of preparing such resistors are also provided.

EP 1 261 241 A1

Description

Background of the Invention

[0001] The present invention relates generally to the field of resistive materials. In particular, the present invention relates to the field of resistive materials suitable for use as embedded resistors in electronic devices.

[0002] Printed circuit boards typically include large numbers of electronic devices which are commonly surface mounted and also additional components which may be present in the form of active layers within each printed circuit board. The requirements for the devices and components in such printed circuit boards are subject to conventional electronic design restraints. In particular, many of the surface mounted devices and other components on such printed circuit boards commonly require coupling with individual resistors in order to achieve their desired function.

[0003] The most common solution to this problem in the prior art has been the use of individual resistors as additional surface mounted components on the printed circuit boards. Design of the printed circuit boards has further required the provision of through-holes in order to properly interconnect the resistors. In this regard, the resistors may be interconnected between any combination of surface devices or components or active components or layers formed on or within the printed circuit boards.

[0004] As a result, the complexity of the printed circuit boards has increased and at the same time the available surface area of the printed circuit boards for other devices has decreased or else the overall size of the printed circuit boards has increased to accommodate necessary surface devices and components including resistors.

[0005] One solution to this has been the use of planar resistors preferably formed on internal layers of the printed circuit boards in order to replace surface mounted resistors as described above while making surface portions of the printed circuit boards free for other uses. For example, U.S. Patent No. 4,808,967 (Rice et al.) discloses a printed wiring board having a support layer, a layer of electrical resistance material adhering to the support layer, and a conductive layer adhering to the electrical resistance layer.

[0006] A problem with certain conventional planar resistors is that the resistance measured in a first direction may differ slightly from the resistance measured in a second direction orthogonal to the first direction. If care is not taken in the manufacture of an electronic device, such as a printed wiring board, such planar resistors may be used in the wrong orientation. In such cases, the actual resistivity of may differ from that desired, thus adversely affecting the performance of the printed wiring board.

[0007] One of the objections to adopting embedded resistor technology in printed wiring board manufacture is that such resistor technology is limited in the range of values that it can provide. Unless large serpentine patterns are employed, a single layer of embedded resistor material is limited to about three decades of values, such as, for example, from 50 ohms to 5,000 ohms. In order to accommodate values above this range one must place discrete resistors on the surface of the printed wiring board, which negates some of the gain from embedding the resistor within the board, or alternatively, use a second sheet of higher resistivity material, which carries a higher cost of materials penalty.

[0008] There is thus a need for a resistive material having a resistivity that is dependent on the orientation of the embedded resistor.

Summary of the Invention

[0009] It has been surprisingly found that printed wiring boards can be prepared having two different sheet-resistivities within a single layer (or plane) of the board. In particular, it has been surprisingly found that multilayer resistors can be prepared.

[0010] In one aspect, the present invention provides a printed wiring board including a resistor embedded within a dielectric material, wherein the resistor includes a resistive material portion including a first resistive material and a second resistive material. Typically, the resistive material portion includes a layer of each of the first and second resistive materials.

[0011] In another aspect, the present invention provides a method of manufacturing a printed wiring board including the step of embedding a resistor within an organic dielectric material, wherein the resistor includes a resistive material portion including a first resistive material and a second resistive material.

[0012] In a further aspect, the present invention provides a resistor having a resistive material portion including a first resistive material and a second resistive material and a pair of electrodes, each electrode being disposed at opposite ends of the resistive material portion.

[0013] In yet another aspect, the present invention provides an electronic device including a resistor and/or a printed wiring board as described above.

Brief Description of the Drawing

[0014] Fig. 1 illustrates one method of manufacturing a multilayer resistor of the invention.

Detailed Description of the Invention

[0015] As used throughout this specification, the following abbreviations shall have the following meanings, unless the context clearly indicates otherwise: ° C = degrees centigrade; ° F = degrees Fahrenheit; nm = nanometer; μm = micron = micrometer; Å = angstrom; Ω = Ohms; Ω/□ = Ohms per square; M = molar; wt % =

percent by weight; and mil = 0.001 inch.

[0016] The terms "printed wiring board" and "printed circuit board" are used interchangeably throughout this specification. Unless otherwis noted, all amounts are percent by weight and all ratios are by weight. All numerical ranges are inclusive and combinable in any order, except where it is obvious that such numerical ranges are constrained to add up to 100%.

[0017] The present invention provides a resistor having a resistive material portion including two or more resistive material layers and a pair of electrodes, each electrode being disposed at opposite ends of the resistive material. The resistive material portion of the present resistors are prepared by providing at least a layer of a first resistive material and a layer of a second resistive material. Additional layers of resistive material may be used, such as three, four, five or more layers. The specific number of layers is determined by the design characteristics of the resistor desired. For example, two layers of resistive materials are required to provide a resistor having 2 possible different resistivities, three layers of resistive materials are required to provide a resistor having 3 possible different resistivities, and so forth.

[0018] One characteristics of the present resistors is that each layer of resistive material in the resistive material portion has a different sheet resistivity from the other resistive material layers. No particular difference in sheet resistivity is required. The sheet resistivities of the different resistive material layers may not be very different or may be different by as much as 10 Ω/□ or greater. Particularly suitable differences in sheet resistivities between the first and second resistive material layers is 25 Ω/□, 50 Ω/□, 100 Ω/□, 250 Ω/□, 500 Ω/□ or greater. In another embodiement, there is a 10, 20, 25, or 50 fold or greater difference in sheet resistivities between the first and second resistive material layers.

[0019] A wide variety of resistive materials are suitable for use in the present invention, including but not limited to, a mixture of a conductive material and a minor amount of a highly resistive (dielectric) material. A very small amount of the highly resistive material, e.g., about 0.1 wt % to about 20 wt %, very profoundly reduces the conductive properties of the conducting material. For example, platinum, though an excellent conductor, when co-deposited with between 0.1 and about 5 wt % silica, serves as a resistor, the resistance being a function of the level of silica co-deposited. Any conductive material is suitable, such as, but not limited to, platinum, iridium, ruthenium, nickel, copper, silver, gold, indium, tin, iron, molybdenum, cobalt, lead, palladium, and the like. Suitable dielectrics include, but are not limited to, metal oxides or metalloid oxides, such as silica, alumina, chromia, titania, ceria, zinc oxide, zirconia, phosphorous oxide, bismuth oxide, oxides of rare earth metals in general, phosphorus, and mixtures thereof.

[0020] Preferred electrically resistive materials are nickel-based or platinum-based, i.e., the major material is nickel or platinum, respectively. Suitable preferred resistive materials are nickel-phosphorus, nickel-chromium, nickel-phosphorus-tungsten, ceramics, conductive polymers, conductive inks, platinum-based materials such as platinum-iridium, platinum-ruthenium and platinum-iridium-ruthenium. Preferred platinum-bas d materials contain from about 10 to 70 mole percent iridium, ruthenium or mixtures thereof, and preferably 2 mole percent to 50 mole percent, calculated relative to platinum being 100 percent. If ruthenium is used alone (without iridium), it is preferably used at between about 2 and about 10 mole percent calculated relative to platinum being 100 percent. If iridium is used alone (without ruthenium), it is preferably used at between about 20 and about 70 mole percent calculated relative to platinum being 100 percent. In the resistive materials in accordance with the invention, the iridium, ruthenium or mixtures thereof exist in both elemental form and in oxide form. Typically, the iridium, ruthenium or mixtures thereof are from about 50 to about 90 mole percent elemental metal and from about 10 to about 50 mole percent oxide (s) of the iridium, ruthenium or mixtures thereof.

[0021] The thickness of each resistive material layer may vary over a wide range. Preferably, each layer of resistive material has a thickness of up to 1 mil. For use in embedded resistors, each layer of resistive material is typically at least about 40 Å thick. In general, the thickness of each resistive material layer is from 40 to 100,000 Å (10 microns), preferably from 40 to 50,000 A, and more preferably from 100 to 20,000 Å.

[0022] While the first resistive material layer may be self-supporting, it is typically too thin to be self-supporting and must be deposited on a substrate which is self-supporting. The resistive materials are typically supported by being disposed on a conductive material substrate, such as a metal foil. Other suitable conductive materials are well known to those skilled in the art. Suitable metal foils include, but are not limited to, copper foil, nickel foil, silver foil, gold foil, and the like as well as alloys thereof. Conductive metal foils suitable for use in the present invention may have a wide range of thicknesses. Typically, such conductive metal foils have nominal thicknesses ranging from 0.0002 to 0.02 inches. Metal foil thicknesses are often expressed in terms of weights. For example, suitable copper foils have weights of from 0.125 to 14 ounces per square foot, more preferably 0.25 to 6 ounces per square foot, and still more preferably from 0.5 to 5 ounces per square foot. Particularly suitable copper foils are those having weights of 3 to 5 ounces per square foot. Suitable conductive metal foils may be prepared using conventional electrodeposition techniques and are available from a variety of sources, such as Oak-Mitsui or Gould Electronics.

[0023] The conductive material substrates may further include a barrier layer. Such barrier layer may be on the first side of the conductive material, i.e. the side nearest the resistive material, the second side of the

conductive layer or on both sides of the conductive layer. Barrier layers are well known to those skilled in the art. Suitable barrier layers include, but are not limited to, zinc, indium, tin, nickel, cobalt, chromium, brass, bronze and the like. Such barrier layers may be deposited electrolytically, electrolessly, by immersion plating, by sputtering, by chemical vapor deposition, combustion chemical vapor deposition, controlled atmosphere chemical vapor deposition, and the like. Preferably, such barrier layers are deposited electrolytically, electrolessly or by immersion plating. In one embodiment, when the conductive layer is a copper foil, it is preferred that a barrier layer is used.

[0024] Following the application of a protective barrier layer, a protective layer of chromium oxide may be chemically deposited on the barrier layer or the conductive material. Finally, a silane may be applied to the surface of the conductive material/barrier layer/optional chromium oxide layer in order to further improve adhesion. Suitable silanes are those disclosed in U.S. Patent No. 5,885,436 (Ameen et al.).

[0025] Each layer of resistive material may be deposited by a variety of means, such as sol-gel deposition, sputtering, chemical vapor deposition, combustion chemical vapor deposition ("CCVD"), controlled atmosphere combustion chemical vapor deposition ("CACCVD"), spin coating, roller coating, silk screening, electroplating, electroless plating and the like. The first layer of resistive material, if not self-supporting, is deposited on the substrate. The second layer of resistive material is deposited on the first resistive material layer. Subsequent layers of resistive material are optionally then deposited. For example, nickel-phosphorus resistive materials may be deposited by electroplating. See, for example, International Patent Application No. WO 89/02212. In one embodiment, it is preferred that the first material is deposited by CCVD and/or CACCVD. The deposition of resistive materials by CCVD and/or CACCVD is well known to those skilled in the art. See, for example, U.S. Patent No. 6,208,234 (Hunt et al.) for a description of such processes and apparatuses used.

[0026] CCVD has the advantages of being able to deposit very thin, uniform layers which may serve as the dielectric layers of embedded capacitors and resistors. The material can be deposited to any desired thickness; however, for forming resistive material layers by CCVD, thicknesses seldom exceed 50,000 Å. (5 microns). Generally film thicknesses are in the 100 to 10,000 A range, most generally in the 300 to 5000 Å range. Because the thinner the layer, the higher the resistance and the less material, e.g., platinum used, the ability to deposit very thin films is an advantageous feature of the CCVD process. The thinness of the coating also facilitates rapid etching in processes by which discrete resistors are formed.

[0027] Although noble metals are conductors, it is found that in depositing noble metals along with relatively minor amounts of oxides, such as silica or alumina, the deposited material becomes highly resistive. Accordingly, metals, such as platinum, containing minor amounts, e.g., 0.1%-5% of an oxide, can serve as resistors in printed circuit boards. For resistive material which is a mixture of a conductive metal and a minor amount of a dielectric material, the metal must be capable of being deposited as a zero valence metal from an oxygen-containing system if the resistive material is to be deposited by CCVD or CACCVD. The criteria for deposition in the zero valence state using a flame is that the metal must have a lower oxidation potential than the lower of the oxidation potential of carbon dioxide or water at the deposition temperature. (At room temperatures, water has a lower oxidation potential; at other temperatures carbon dioxide has a lower oxidation potential.) Zero valence metals which can be readily deposited by CCVD are those having oxidation potentials about equal to silver or below. Thus, silver, gold, platinum and iridium can be deposited by straight CCVD. Zero valence metals having somewhat higher oxidation potentials may be deposited by CACCVD which provides a more reducing atmosphere. Nickel, copper, indium, palladium, tin, iron, molybdenum, cobalt, and lead are best deposited by CACCVD. Herein, metals also include alloys that are mixtures of such zero-valence metals. Silicon, aluminum, chromium, titanium, cerium, zinc, zirconium, magnesium, bismuth, rare earth metals, and phosphorous each have relatively high oxidation potentials, such that if any of the metals mentioned above are codeposited with the appropriate precursors for the dielectric dopants, the metals will deposit in the zero valence state and the dopant will deposit as the oxide. Thus, even when no flame is used the dielectric needs to have a higher oxidation, phospidation, carbidation, nitrodation, or boridation potential, to form the desired two phases.

[0028] For more oxygen-reactive metals and alloys of metals, CACCVD may be the process of choice. Even if the metal can be deposited as a zero valence metal by straight CCVD, it may be desirable to provide a controlled atmosphere, i.e., CACCVD, if the substrate material on which it is to be deposited is subject to oxidation. For example, copper and nickel substrates are readily oxidized, and it may be desired to deposit onto these substrates by CACCVD.

[0029] Another type of resistive material which can be deposited as a thin layer on a substrate by CCVD is "conductive oxides". In particular, $Bi_2Ru_2O_7$ and $SrRuO_3$ are conductive oxides which may be deposited by CCVD. Although these materials are "conductive", their conductivity is relatively low when deposited in amorphous state; thus, a thin layer of such mixed oxides can be used to form discrete resistors. Like conductive metals, such "conductive oxides" may be doped with dielectric materials, such as metal or metalloid oxides, to increase their resistivity. Such mixed oxides may be deposited either as amorphous layers or as crystalline layers, amorphous layers tending to deposit at low depo-

sition temperatures and crystalline layers tending to deposit at higher deposition temperatures. For use as resistors, amorphous layers ar generally preferred, having higher resistivity than crystalline materials. Thus, while these materials are classified as "conductive oxides" in their normal crystalline stat , the amorphous oxides, even in un-doped form, may produce good resistance. In some cases it may be desired to form low resistance, 1 to 100 Ω, resistors and a conduction-enhancing dopant, such as platinum, gold, silver, copper or iron, may be added. If doped with dielectric material, e.g., metal or metalloid oxides, to increase resistivity of the conducting oxides, or conduction-enhancing material to decrease resistivity of the conducting oxides, such homogeneously mixed dielectric or conduction-enhancing material is generally at levels between 0.1 wt % and 20 wt % of the resistive material, preferably at least 0.5 wt %.

[0030] There are a variety of other "conducting materials" which though electrically conducting, have sufficient resistivity to form resistors in accordance with the present invention. Examples include yttrium barium copper oxides and $La_{1-x}Sr_xCoO_3$, $0 \leq x \leq 1$, e.g., $x = 0.5$. Generally, any mixed oxide which has superconducting properties below a critical temperature can serve as electrically resistive material above such critical temperature. Deposition of such a variety of resistive materials is possible with proper selection of precursors selected from those described herein above.

[0031] To produce a metal/oxide resistive material film using a CCVD or CACCVD process, a precursor solution is provided which contains both the precursor for the metal and the precursor for the metal or metalloid oxide. For example, to produce platinum/silica films, the deposition solution contains a platinum precursor, such as platinum(II)-acetylacetonate or diphenyl-(1,5-cyclooctadiene) platinum (II) [Pt(COD)] and a silicon-containing precursor, such as tetraethoxysilane. Suitable precursors for iridium and ruthenium include, but are not limited to, tris (norbornadiene) iridium (III) acetyl acetonate ("IrNBD"), and bis (ethylcyclopentadienyl) ruthenium (II). The precursors are mixed generally according to the ratio of metal and enhancing material to decrease the resistivity of the material being deposited, an additional precursor is provided so as to produce minor amounts of the metal oxide or metalloid oxide, e.g., between 0.1 and 20 wt %, preferably at least about 0.5 wt %, of the deposited doped conducting metal oxide. The precursors typically are co-dissolved in a single solvent system, such as toluene or toluene/propane to a concentration (total of platinum, iridium, and/or ruthenium precursors) of from about 0.15 wt% to about 1.5 wt%. This solution is then typically passed through an atomizer to disperse the precursor solution into a fine aerosol and the aerosol is ignited in the presence of an oxidizer, particularly oxygen, to produce the platinum and iridium, ruthenium or mixture thereof zero valence metals(s) and oxide(s). See, e.g. U.S. Patent No. 6,208,234 B1 (Hunt et al.), herein incorporated by reference, for a more complete description of the CCVD process.

[0032] A wide variety of materials are suitable to form as the second resistive material layer on the first resistive material. The only requirement for such second resistive material layer is that it be different from th first material and posses a sheet resistivity that is different from the sheet resistivity of the first resistive material layer. Any of the resistive materials described above as being suitable as a first resistive material layer are also suitable for use as a second material.

[0033] The present structure having two or more resistive materials, particularly two or more layers of resistive materials, are suitable for the manufacture of resistors, and in particular thin film, embeddable resistors useful in printed wiring board manufacture. Thin film resistors typically have a total thickness of the resistive material portion of 4 μm or less, preferably 2 μm or less, more preferably 1 μm or less and even more preferably 0.5 μm or less.

[0034] Resistors typically include a pair of electrodes, each electrode being disposed at opposite ends of a resistive material portion. Such electrodes may be provided in a variety of ways, such as by formation directly on the resistive material or directly formed from an underlying conductive substrate. By way of example, areas of the resistive material to receive the electrode may be catalyzed so that electrodes are deposited, formed, or adhered only to those catalyzed areas. Alternatively, areas that are not to receive the electrode may be masked off, such as by a resist, and the electrode deposited or formed on or otherwise adhered to the unmasked areas.

[0035] Suitable electrodes may be formed by any conductive material such as a conductive polymer or a metal. Exemplary metals include, but are not limited to, copper, gold, silver, nickel, tin, platinum, lead, aluminum and mixtures and alloys thereof. "Mixtures" of such metals include non-alloyed metal mixtures and two or more layers of individual metals as in a multilayer electrode. An example of a multilayer electrode is copper having a layer of silver or a layer of nickel on the copper followed by a layer of gold. Such electrodes are typically formed by deposition of a conductive material. Suitable deposition methods include, but are not limited to, electroless plating, electrolytic plating, chemical vapor deposition, CCVD, CACCVD, screen printing, ink jet printing, roller coating and the like. When a conductive paste is used to form the electrode, it is suitably applied by screen printing, ink jet printing, roller coating and the like.

[0036] As described above, when the first resistive material is not self-supporting, it is typically applied to a substrate. Conductive substrates are particularly suitable for subsequent formation of resistors, particularly thin film resistors, as the conductive substrates can be used to form the pair of electrodes. This is generally accomplished using a photoresist which is used to form a resist pattern over the layer of resistive material and using an appropriate etchant to remove the resistive ma-

terial in areas not covered by the resist. For metal/oxide resistive material layers, the etchant chosen is an etchant for the metal component of the resistive material. Typically such etchants are acids or Lewis acids, e.g., $FeCl_3$ or $CuCl_2$ for copper. Nitric acid and other inorganic acids (e.g., sulfuric, hydrochloric, and phosphoric) may be used to etch nickel, a variety of other metals which may be deposited as well as conductive oxides.

[0037] Noble metals, by their non-reactive nature, are difficult to etch. Aqua regia is a suitable etchant for metals, particularly noble metals, in printed circuit board processes. Aqua regia is made from two well-know acids: 3 parts concentrated (12M) hydrochloric acid (HCl) and 1 part concentrated (16M) nitric acid HNO_3. Thus, the molar ratio of hydrochloric acid to nitric acid is 9:4, although slight variations from this ratio, i.e., 6:4 to 12: 4 would be acceptable for etching purposes in accordance with the invention. Because of its corrosive nature and limited shelf life, aqua regia is not sold commercially, but must be prepared prior to use. To reduce its corrosiveness, the aqua regia may be diluted with water up to about a 3:1 ratio of water to aqua regia. On the other hand, the noble metals, such as platinum, are not etched by many of the materials suitable for etching copper, such as $FeCl_3$ or $CuCl_2$, thereby allowing for a variety of selective etching options in forming the present resistors. The speed of etching will depend upon several factors including the strength of the aqua regia and the temperature. Typically, aqua regia etching is conducted at a temperature of 55 to 60° C, although this may be varied depending upon the application.

[0038] By way of example, the circuitization process begins with a conductive foil, such as a copper foil, to which a layer of a first electrically resistive material has been deposited, such as by electroplating, CCVD or CACCVD. A second electrically resistive material layer is then formed on the first resistive material layer by any of the methods described above to form a multilayer resistive material.

[0039] In one embodiment, photoresist layers are applied to both sides, i.e. to the resistive material portion and to the conductive foil. The photoresist covering the resistive material portion is exposed to patterned actinic radiation while the photoresist covering the conductive foil is blanket-exposed to actinic radiation. The photoresists are then developed, giving a structure with a patterned photoresist layer covering the resistive material portion and the blanket-exposed photoresist layer protecting the conductive foil.

[0040] The resistive material layer is then selectively etched from areas where the photoresist had been removed. Subsequently, the remaining photoresist is stripped.

[0041] Following this, an organic laminate such as a polyimide or a glass-filled epoxy prepreg is applied to the resistive material side. The laminate protects the now-patterned resistive material layer from further processing and subsequently supports patches of the resistive material layer when portions of the conductive foil is subsequently removed from the other side of the resistive material layer.

[0042] Next, a photoresist layer is applied to the conductive foil. This is imaged with patterned actinic radiation and developed. Following this, th conductiv foil is etched with an etchant which selectively etches the conductive foil but which does not etch the resistive material layer. Stripping of the photoresist leaves the resistor which may subsequently be embedded in an organic dielectric material, such as a B-staged dielectric material including, but not limits to, epoxies, glass-filed, polyimides and the like.

[0043] As a variation of this process, it should be noted that if an etchant is used which selectively etches the electrically resistive material layer but does not etch or only partially etches the conductive foil, the use of a resist layer on the conductive foil is not necessary.

[0044] In an alternate embodiment, the resistor is laminated to or otherwise adhered to an organic dielectric material prior to circuitization. Such a process is illustrated in Fig. 1.

[0045] Referring to Fig. 1, a first resistive material layer **10**, such as a nickel-phosphorus layer, is deposited, such as by electroplating, on a conductive foil **5**. Such conductive foil **5** is typically copper. A second resistive material layer **15** is then deposited on the first resistive material layer **10**. An exemplary second resistive material layer **15** is a platinum-iridium layer which is deposited by CCVD to provide resistive material structure **50**. By "resistive material structure" it is meant a substrate, preferably a conductive substrate, having a first resistive material layer disposed on the substrate and a second resistive material layer disposed on the first resistive material layer, wherein the conductive substrate, first resistive material layer and second resistive material layer are coextensive. In this example, the nickel-phosphorus resistive material layer has a sheet resistivity of 25 Ω/□ and the platinum-iridium resistive material layer has a sheet resistivity of 1000 Ω/□.

[0046] Next, an organic dielectric material **20**, such as an epoxy laminate material, is laminated to the second resistive material layer **15**. A photoresist **25**, particularly a dry film photoresist, is then applied to the conductive foil **5**. Photoresist **25** is then imaged and developed to provide the designed pattern. Conductive foil **5** is next removed from the areas bared of resist, such as by etching within cupric chloride.

[0047] One of the advantages of the present resistors is that their resistivity may be selected by appropriate selection of the resistive material layer to remain during formation of the resistor. This is further illustrated in Fig. 1 which shows an embodiment where two resistors, each having a different resistivity, are prepared from the same resistive material structure **50**. First resistive material **10** may be removed from the areas bared of conductive foil **5**. In the case of nickel-phosphorus, such material may be removed by etching with copper sulfate.

The second resistive material layer **15** is also removed from the areas that are to be free of resistive material, such as areas **45** between resistor structures.

[0048] In a next step, another photoresist **30**, such as dry film photoresist, is applied to the conductive foil side of the structure. Photoresist **30** is then imaged and developed to provide the desired pattern of conductive traces (including electrodes). Conductive foil **5** is again removed from areas bared of resists, to provide resistor **40**, which in the above description has a sheet resistivity of 25 Ω/□ due to the presence of the first resistive material layer **10**. Resistor **35** having a different resistivity is obtained by selectively etching or removing the first resistive material layer **10** and leaving the second resistive material layer **15**. In the above example, resistor **35** has a sheet resistivity of 1000 Ω/□.

[0049] When referring herein to "etching", the term is used to denote not only the common usage in this art where a strong chemical dissolves or otherwise removes the material of one of the layers, e.g., nitric acid dissolves nickel, but also physical removal, such as laser removal and removal by lack of adhesion. In this regard, and in accordance with an aspect of this invention, it is found that resistive materials, such as doped nickel and doped platinum, deposited by CCVD or CACCVD are porous. The pores are believed to be small, typically of a diameter of a micron or less, preferably of a diameter of 50 nanometers or less (1000 nm = 1 μm). Nevertheless, this permits liquid etchants to diffuse through the electrically resistive material layer and, in a physical process, destroy the adhesion between the resistive material layer and the underlying layer. For example, if the conductive foil layer is copper and the resistive material layer is doped platinum, e.g., platinum/silica, or doped nickel, e.g., Ni/PO_4, cupric chloride could be used to remove exposed portions of the resistive material layer. The cupric chloride does not dissolve either platinum or nickel, but the porosity of the resistive material layer allows the cupric chloride to reach the underlying copper. A small portion of the copper dissolves and the exposed portions of the electrically resistive layer by physical ablation. This physical ablation occurs before the cupric chloride etches the underlying copper layer to any significant extent.

[0050] If copper is the conductive material layer, it is sometimes advantageous to use copper foil that has been oxidized, which is commercially available. An advantage of an oxidized copper foil is that a dilute hydrochloric acid ("HCl") solution, e.g., ½ %, dissolves copper oxide without dissolving zero valence copper. Thus, if the electrically resistive material layer is porous, such that the dilute HCl solution diffuses therethrough, HCl can be used for ablative etching. Dissolving the surface copper oxide destroys the adhesion between the copper foil and the electrically resistive material layer.

[0051] To minimize processing steps, the photoresists used can themselves be embeddable in materials, such as a permanent etch resist such as that available from Shipley Company, Marlborough, Massachusetts. Then both sides can be processed simultaneously if the etchant does not or only partially etches the conductor. In particular, only the resistor material side photoresist needs to be embeddable and the conductor side can be removed as a final processing step. Alternatively, the photoresists used on the conductor material side can be selected such that it is not removed with a specific stripper used to remove the resistor material side photoresist. Embedable photoresist may decrease tolerance losses due to particular undercutting of resistor material which under cut material will ablate once the photoresist is removed.

[0052] To be practically removable by an ablative technique, the resistive material layer must generally be sufficiently porous to an etchant which does not dissolve the electrically resistive material but sufficiently attacks the surface of the underlying material such as to result in loss of interfacial adhesion and ablation of the electrically conductive material within about 2 to 5 minutes. At the same time, such etchant must not substantially attack the underlying material, e.g., copper foil, during the etching period as such would cause excessive undercutting or loss of mechanical strength (i.e., reduce handleability).

[0053] In another embodiment, the present invention provides a multi-layer structure which comprises an insulating substrate, a resistive material patch having two or more layers of different resistive material, e.g., platinum/silica formed by CCVD and a nickel-phosphorus layer and a conductive patch (or electrodes), e.g., copper. Preferably, both the resistive material patches and the electrical connection conductive patches are formed by photoimaging techniques. In such structure, the first and second resistive material layers may be coextensive or, alternatively, the first resistive material layer may be coextensive with the conductive patches, i.e. electrode pair.

[0054] The multi-layer structure could be patterned using photoimaging technology. In one procedure, the conductive material layer would be covered with a resist, the resist patterned by photoimaging techniques, and, in the exposed areas of the resist, both the conductive material layer and the underlying resistive material layer be etched away, e.g., with aqua regia to give a structure of having a patterned structured resistive material patch (and a patterned conductive material patch or electrode). Next, a second photoresist would be applied, photoimaged, and developed. This time, only the exposed portions of the conductive material patch would be etched away by etchant which would selectively etch the conductive layer, but not the resistive material patch, i.e., $FeCl_3$ or $CuCl_2$ in the case of copper as the conductive material layer and platinum/silica as the electrically resistive material. In an alternate procedure, a patterned resist layer would be formed, exposed portions of the conductive material layer etched away, e.g., with $FeCl_3$, a further patterned resist layer formed, and then the ex-

posed areas of the resistive material layer etched away with aqua regia so as to form the electrical contacts. By either procedure, discrete thin layer resistors are formed by conventional photoimaging techniques common to printed circuitry formation.

[0055] While the present resistors could be at the surface of a printed circuit board device, the resistors will, in most cases, be embedded within a multi-layer printed circuit board, for example where the resistor, which was formed on an organic dielectric substrate, such as polyimide or epoxy, is embedded within additional embedding insulating material layers, such as epoxy/fiberglass prepreg material.

[0056] Structures containing the present two or more layers of resistive materials may be used in the manufacture of electronic devices, and particularly as resistors embedded in a dielectric material. Thus, the present invention provides an electronic device including a resistor having two or more layers of resistive material, wherein each layer of resistive material is different from the other layers of resistive material. Suitable electronic devices include, but are not limited to printed wiring boards, computers, microprocessors, telecommunications equipment such as mobile or cellular telephones, and the like.

[0057] In particular, the present structures are suitable for embedding in a dielectric material in the manufacture of printed wiring boards. Therefore, the present invention also provides an electronic device including a printed wiring board Including a resistor having a resistive material portion having two or more layers of resistive material, wherein each layer of resistive material is different from the other layers of resistive material. Also provided by the present invention is an electronic device including a resistor, the resistor including a pair of electrodes and a resistive material portion, the resistive material portion including two or more layers of resistive material, wherein each layer of resistive material is different from the other layers of resistive material.

[0058] When the resistive material portion of any of the above described resistors includes two layers of resistive material, such layers may be coextensive or the first resistive material layer may be coextensive with the pair of electrodes. When three layers of resistive material are used, all three layers may be coextensive, the first resistive material layer may be coextensive with the pair of electrodes while the second and third resistive material layers are coextensive, or, alternatively, the first and second resistive material layers may be coextensive with the pair of electrodes.

[0059] In general, a sheet of the present resistive material structure is laminated to a sheet of organic dielectric material. The resistive material structure is then etched (such as following photolithography) as described above to form any number of individual resistors within the same plane. It will be appreciated by those skilled in the art that a number of such planes of resistors may be present within a multiplayer printed wiring board.

Claims

1. A resistor comprising a resistive material portion comprising a first resistive material and a second resistive material, and a pair of electrodes, each electrode being disposed at opposite ends of the resistive material portion.

2. The resistor of claim 1 wherein the first resistive material and second resistive material have a difference in sheet resistivities of 10 Ω/□ or greater.

3. The resistor of any one of claims 1 to 2 wherein at least one of the first and second resistive materials is platinum-based or nickel-based.

4. The resistor any one of claims 1 to 3 wherein the electrodes comprise copper, gold, silver, nickel, tin, platinum, lead, aluminum, or mixtures or alloys thereof.

5. A printed wiring board comprising a resistor of any one of claims 1 to 4 embedded within an organic dielectric material.

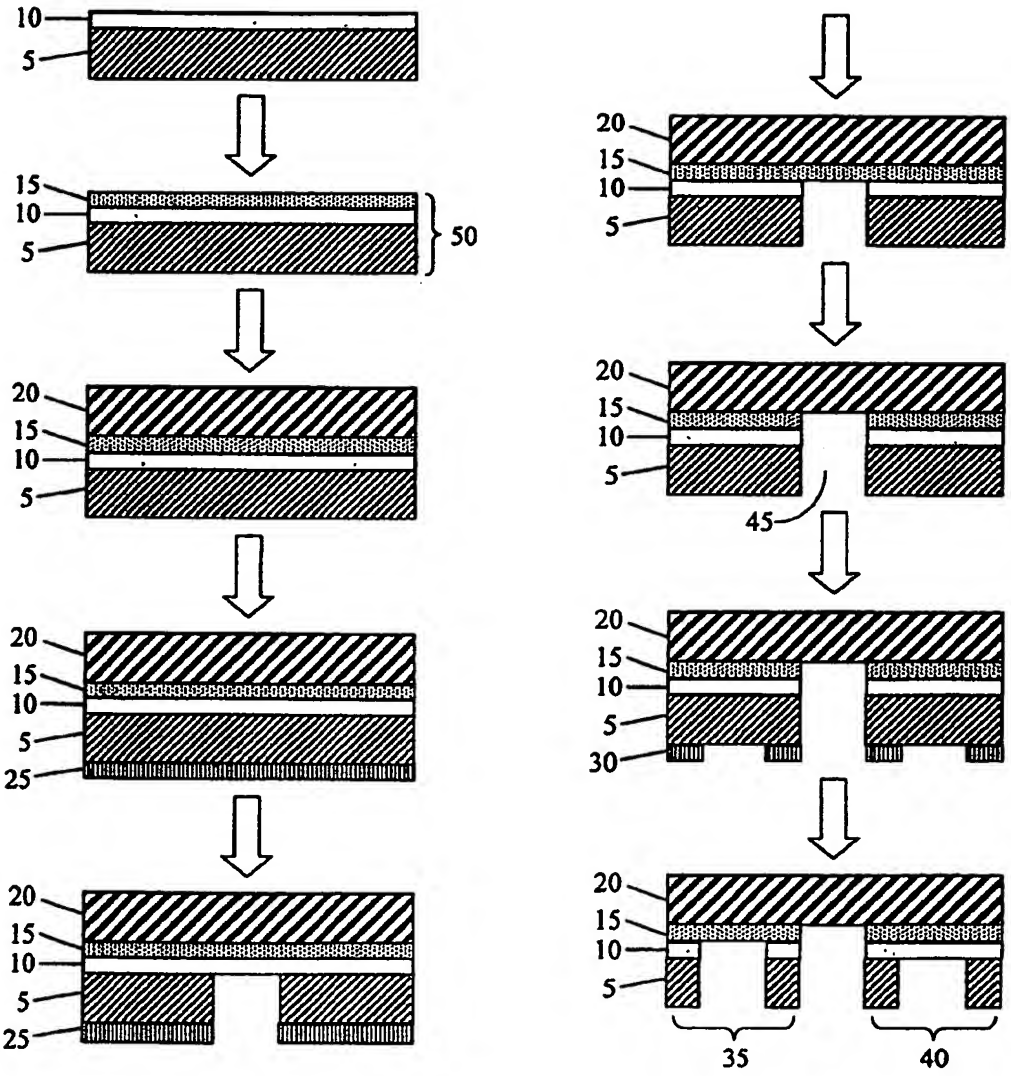
6. A method of manufacturing a printed wiring board comprising the step of embedding a resistor any one of claims 1 to 4 within an organic dielectric material.

7. A structure suitable for forming a resistor comprising a conductive substrate, a first resistive material layer disposed on the conductive substrate, and a second resistive material layer disposed on the first resistive material layer.

8. The structure of claim 9 wherein the first resistive material layer and second resistive material layer have a difference in sheet resistivities of 10 Ω/□ or greater.

9. A method of manufacturing a printed wiring board comprising the step of embedding a structure of any one of claims 7 to 8 within an organic dielectric material.

Fig. 1


10
5
15
10
5
50
20
15
10
5
20
15
10
5
25
20
15
10
5
25
20
15
10
5
20
15
10
5
45
20
15
10
5
30
20
15
10
5
35
40

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 3403

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 3 896 284 A (HOLMES EDWARD S B) 22 July 1975 (1975-07-22) * claim 2 *	1	H05K1/18 H01C7/00
X	EP 0 540 820 A (DEUTSCHE AEROSPACE) 12 May 1993 (1993-05-12) * abstract; claims 1,6,7; figure 1 * * column 2 *	1-4	
X	EP 0 657 898 A (KONINKL PHILIPS ELECTRONICS NV) 14 June 1995 (1995-06-14) * abstract; claims 1,3; figure 3B *	1,3,4	
Y	EP 0 330 210 A (GOULD INC) 30 August 1989 (1989-08-30)	1-9	
X	* page 15-17; claims 133-136; figures 2,4 *	2-6,8,9	
Y	EP 1 096 838 A (MICROCOATING TECHNOLOGIES) 2 May 2001 (2001-05-02) * column 1, line 0-12 * * column 2, line 40-55 * * column 6, line 15-30 *	1-9	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01C H05K H01L H01G
X	* claims 1,17 *	2-6,8,9	
Y	EP 1 093 327 A (DU PONT) 18 April 2001 (2001-04-18) * abstract; claims 1,3 *	5,6,9	
A	US 3 886 578 A (ARTS MARCUS ET AL) 27 May 1975 (1975-05-27) * the whole document *	1-9	
X	* claim 1 *	2	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	24 September 2002	Dessaux, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 3403

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

24-09-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3896284 A	22-07-1975	US 3864825 A	11-02-1975
EP 0540820 A	12-05-1993	DE 4136198 A1	06-05-1993
		EP 0540820 A1	12-05-1993
EP 0657898 A	14-06-1995	BE 1007868 A3	07-11-1995
		DE 69409614 D1	20-05-1998
		DE 69409614 T2	05-11-1998
		EP 0657898 A1	14-06-1995
		JP 7201529 A	04-08-1995
		US 6097276 A	01-08-2000
EP 0330210 A	30-08-1989	AU 3075289 A	31-08-1989
		BR 8900871 A	17-10-1989
		CN 1040298 A ,B	07-03-1990
		DD 287140 A5	14-02-1991
		DD 298292 A5	13-02-1992
		DD 295493 A5	31-10-1991
		EP 0330210 A2	30-08-1989
		EP 1011111 A1	21-06-2000
		IN 171824 A1	23-01-1993
		JP 1309301 A	13-12-1989
		JP 3022969 B2	21-03-2000
		KR 9207430 B1	31-08-1992
		US 5243320 A	07-09-1993
EP 1096838 A	02-05-2001	US 6212078 B1	03-04-2001
		CN 1311625 A	05-09-2001
		EP 1096838 A2	02-05-2001
		JP 2001210956 A	03-08-2001
		US 2001012600 A1	09-08-2001
EP 1093327 A	18-04-2001	US 6317023 B1	13-11-2001
		EP 1093327 A2	18-04-2001
		JP 2001160672 A	12-06-2001
		US 2002028284 A1	07-03-2002
US 3886578 A	27-05-1975	AU 465334 B	25-09-1975
		AU 6486474 A	21-08-1975
		BE 811337 A1	17-06-1974
		CA 1019039 A1	11-10-1977
		DE 2402709 A1	05-09-1974
		FR 2219606 A1	20-09-1974
		GB 1408122 A	01-10-1975
		JP 1038251 C	24-03-1981
		JP 49117959 A	11-11-1974

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 3403

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

24-09-2002

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 3886578 A		JP 55029562 B	05-08-1980
		NL 7401619 A	28-08-1974
		SE 387038 B	23-08-1976

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82